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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/650,719	05/20/96	MAILLOUX J	95-0653

021186 TM02/0716
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EXAMINER	
KIM, H	
ART UNIT	PAPER NUMBER
2185	28

DATE MAILED: 07/16/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
08/650,719	Mailloux et al,
Examiner	**Group Art Unit**
H. Kim	2185

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 (three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on 5/2/01.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-9, 33-35, 46, 48-50, 59-61, 63-64 is/are pending in the application.

Of the above claim(s)_____ is/are withdrawn from consideration.

☐ Claim(s)_____ is/are allowed.

☒ Claim(s) 1-9, 33-35, 46, 48-50, 59-61, 63-64 is/are rejected.

☐ Claim(s)_____ is/are objected to.

☐ Claim(s)_____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on_____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on_____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)_____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:_____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 14

☐ Interview Summary, PTO-413

☐ Notice of References Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other_____

Office Action Summary

Detailed Action

1. Claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 are presented for examination. This office action is in response to the Amendment filed on /5/2/01.

2. Applicant is requested to submit a search report for each of PCT/US95/16984 filed 12/22/1995 and PCT/US95/16656 filed 12/21/1995 which are listed on the IDS submitted on 6/28/1999 because the search reports are not readily available to the Examiner.

DOUBLE-PATENTING

3. The non-statutory double patenting rejection, whether of the obviousness-type or non-obviousness-type, is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent. *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); and *In re Goodman*, 29 USPQ2d 2010 (Fed. Cir. 1993).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(b) and (c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.78(d).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 59-60 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 36 of copending Application No. 08/984,563. Although the conflicting claims are not identical, they are not patentably distinct from each other because both sets of claims are related to a method of accessing a storage device, comprising: a first address, burst and pipelined mode, selecting inputting and outputting information, selecting a burst mode and a pipelined mode, utilizing a second address to access data in a memory. Both sets of claims recited similar inventive concept of accessing a memory in burst and pipelined mode except: Claims 59-60 of the present invention comprises less specific steps than as claimed in the Application No. 08/984,563. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize teaching of 08/984,563 and modify an external row address to a first address and a first external column address to a second address of the copending application to arrive invention of the present application.

5. Claim 61 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 59 of copending Application No. 08/984,561. In view of Although the conflicting claims are not identical, they are not patentably distinct from

each other because both sets of claims are related to a method of accessing a storage device in burst and pipelined mode. Claims 61 of the present invention comprises less comprises less elements than as claimed in the Application No. 08/984,563. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to delete additional limitations of maintaining a first enabling signal in an active state of the copending application to arrive invention of the present application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Objections

6. Claim 61 is still objected to because of the following informalities:

As to claim 61, it is unclear to the Examiner how to provide a new external addresses while in the burst mode of operation when you are already in a pipeline mode of operation (see lines 3-6). Also it is unclear how to generate at least one subsequent internal address patterned after the initial external address while in the pipelined mode of operation while in the burst mode of operation (lines 10-11). It appears that "burst mode" and "pipelined mode" are inadvertently exchanged. Also it appears that there is no support in the specification.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

8. Claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 are rejected under 35 USC 102(e) as being anticipated by *Manning*, U.S. Patent 5,610,864.

As to claim 1, *Manning* discloses the invention as claimed. *Manning* discloses an asynchronously accessible storage device (Fig. 1 and EDO constitutes asynchrous memory, col. col. 6 lines 14-16) comprising mode circuitry to select between a burst mode (col. 6 lines 14-34 and col. 7 lines 43-54) and a pipelined mode (col. 5 lines 43-50, "the current invention include a pipelined architecture" and "switching between standard fast page mode (non-EDO) and burst mode" read on this limitation, in other words, Manning discloses mode circuitry to select between fast page pipeline and burst); and circuitry operable in either the burst mode or the pipelined mode coupled to the mode selection circuity and configure to select between two modes.(Fig. 1 Ref. 40 and col. 6 lines 14-16 & col. 5 lines 41-50).

As to claim 50, Manning further discloses a microprocessor (Fig. 11 Ref. 112). Manning also disclose a system clock (col. 8 line 46) in the microprocessor to operate the processor.

As to claim 2, Manning further discloses the burst mode and the pipelined mode are EDO modes of operation (col. 5 lines 41-50, col. 6 lines 14-34 and col. 7 lines 43-54).

As to claim 3, Manning further discloses the pipelined mode is an EDO mode (col. 5 lines 41-50, col. 6 lines 14-34 and col. 7 lines 43-54).

As to claim 4, Manning further discloses the burst mode is and EDO mode (col. 6 line 15).

As to claim 5, Manning further discloses the mode circuitry includes a buffer, the buffer for storing an address (Fig. 1 Refs. 18, 22, and 30).

As to claim 6, Manning further discloses the mode circuitry includes at least one counter for incrementing the address (Fig. 1 Ref. 26 and col 5 lines 51-62).

As to claim 7, Manning further discloses the mode circuitry includes receiving an external address (Fig. 1 Ref. 16 and col. 4 lines 16-28).

As to claim 8, Manning further discloses the mode circuitry includes a buffer, the buffer for storing an address (Fig. 1 Refs. 18, 22, and 30).

As to claim 9, Manning further discloses the mode circuitry includes multiplexed device for providing an internally generated address to the storage device (Fig. 1 Refs. 26 and 30 and col. 5 lines 51-62 & col. 3 lines 20-23, selection of external or internal address reads on this limitation).

As to claims 33, 59, and 60, *Manning* discloses a method for accessing a storage device (Fig. 1), comprising: receiving a first address to the storage device (Fig. 2 ROW); selecting between an asynchronously accessible (Fig. 1 and EDO constitutes asynchrous operation, col. col. 6 lines 14-16) burst mode (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipelined mode (col. 5 lines 43-50) of operations of the storage device; selecting between outputting information from the storage device and inputting to the storage device (Fig. 2 /WE, read and write operations read on this limitation); obtaining a second address to the storage device (Fig. 2 /COL), and asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second addresses (Fig. 2, DQ and col. 5 lines 41-50, col. 6 lines 14-26 & col. 7 lines 43-54).

As to claim 34, Manning further discloses a step of switching between the pipelined mode and burst mode (col. 5 lines 41-50, col. 6 lines 14-16 and col. 5 lines 42-50).

As to claim 35, Manning further discloses the second address is an external address (Fig.

1 Refs 16 and 30 and col. 4 lines 16-28).

As to claim 46, *Manning* discloses a method for accessing several different locations in an asynchronously a storage device (Fig. 1 and EDO constitutes asynchrous operation, col. col. 6 lines 14-16), comprising: selecting a pipelined mode of operation (col. 5 lines 42-50); providing a new external addresses for every access associated with accessing the asynchronously-accessible memory device while in the pipelined mode of operation (col. 5 lines 42-50, "where memory accesses are performed sequentially" and "one access per cycle" read on this limitation); switching a burst mode of operation (col. 6 lines 14-26 and col. 7 lines 43-54); providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the burst mode of operation (col. 5 lines 51-62 and col. 8 line 67); and generating at least one subsequent internal address patterned after the initial external address while in the burst mode of operation (col. 5 lines 51-62 and col. 8 line 67).

As to claims 48 and 49, Manning further discloses column, row, application, fixed access based switching (col. 5 line 42 thru col. 6 line 34) for the burst mode and the pipelined mode.

As to claim 61, *Manning* discloses a method for accessing several different locations in an asynchronously a storage device (Fig. 1 and EDO constitutes asynchrous operation, col. col. 6 lines 14-16), comprising: selecting a pipelined mode of operation (col. 5 lines 42-50); providing a

new external addresses for every access associated with accessing the asynchronously-accessible memory device while in the pipelined mode of operation (col. 5 lines 42-50, definition of the pipeline "where memory accesses are performed sequentially" and "one access per cycle" reads on this limitation); switching a burst mode of operation (col. 6 lines 14-34 and col. 7 lines 43-54); providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the burst mode of operation (col. 5 lines 51-62 and col. 8 line 67); and generating at least one subsequent internal address patterned after the initial external address while in the burst mode of operation (col. 5 lines 51-62 and col. 8 line 67).

As to claim 63, *Manning* discloses a storage device, comprising; an array of memory cells (col. 4 lines 13-15); mode circuitry for receiving a burst/pipeline signal (col. 5 lines 41-50, col. 6 lines 14-34 & col. 7 lines 43-54); and operation circuitry operable in a burst or a pipeline mode of operation depending upon the burst/pipeline signal, the operation circuitry switchable between burst and pipeline modes of operation (col. 5 lines 41-50, col. 6 lines 14-34, and col. 7 lines 43-54).

As to claim 64, *Manning* discloses a memory circuit, comprising; an array of memory cells (col. 4 lines 13-15); burst/pipeline selection circuitry for determining a burst or a pipeline mode of operation of the memory circuit (col. 5 lines 41-50, col. 6 lines 14-34 & col. 7 lines 43-54); and mode circuitry capable of operation in either a burst mode or a pipeline mode of operation, and

switchable between burst and pipeline modes of operation (col. 5 lines 41-50, col. 6 lines 14-34, and col. 7 lines 43-54).

Response to Amendment

9. Applicant's arguments filed on 5/2/01 have been fully considered but they are not persuasive.

Applicant's argument on page 4 that the reference does not disclose selecting between a burst mode and a pipeline modes of operations is not considered persuasive.
Manning discloses this limitation ("the current invention include a pipelined architecture" (col. 5 lines 43-49) and "switching between standard fast page mode (non-EDO) and burst mode" (see col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55) read on this limitation, in other words, Manning discloses a mode circuitry to select between fast page pipeline and burst since Manning discloses that the current invention include a pipelined architecture (col. 5 lines 43-49) which would increase accessing speed. Therefore, broadly written claims are disclose by the references cited. Also page 77 in "Rossini, Pentium, PCI-ISA, Chip set", Symphony Laboratories, June 1995 (IDS filed on 6/28/1999) also discloses selecting between burst and burst pipeline in SRAM.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

12. Applicants are requested to number each line of each claim starting with line number one to provide easier communication in the future.

13. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

14. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

15. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can

normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Do Yoo, can be reached on (703) 308-4908.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

16.. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-6296 or (703) 308-6165

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Patent Examiner
July 15, 2001